JPEG Encoder IP Core Setup Guide on Intel Quartus

VISENGI

Hardware & Software Engineering

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Revision History

Rev.	Date	Description
1.0	2014-11-20	Initial documentation
1.1	2015-08-06	Describe AXI interfaces' endianness. Update optional AXI4-ST output width.
1.2	2018-11-02	Update to latest Intel Quartus JPEG/X IP blocks

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Setting Up

The following guide describes how to set up the Intel Quartus Qsys drag'n'drop instance deliverables for **implementing VISENGI's JPEG Encoder IP core on Intel projects**.

Requirements

- Intel Quartus 14.0 or newer (Web or Subscription Edition).

List of deliverables

Three versions of the same VISENGI JPEG Encoder (JPEGE) IP core are delivered, the only difference between versions being the bus used on the Data I/O Interface (for Pixel Input and Coded Output):

- **jpeg[x]_encoder_hw.tcl:** JPEG Encoder instance description, with AXI4-Lite for the configuration interface and AXI3* (memory-mapped) interfaces for Pixel Input and Coded Output.

- **jpeg[x]_encoder_st_hw.tcl:** JPEG Encoder instance description, with AXI4-Lite for the configuration interface and AXI4-Stream interfaces for Pixel Input and Coded Output. The pixel input is compatible with AXI4-ST Video IP interfaces as defined by Xilinx in user guide UG934.

- **jpeg[x]_encoder_stin_hw.tcl:** JPEG Encoder instance description, with AXI4-Lite for the configuration interface, AXI3* for Coded Output, and AXI4-Stream interface only for Pixel Input. The pixel input is compatible with AXI4-ST Video IP interfaces as defined by Xilinx in user guide UG934.

*AXI3 buses are forward compatible towards AXI4 interconnects.

Note: the optional "x" in the component names above indicates that the JPEG Encoder may be capable Extended Baseline mode too (i.e. > 24bpp), if the IP core licensed is "JPEG Extended".

Evaluation limits

If these files were downloaded from VISENGI's website, their purpose is to show how simple it is to embed a hardware JPEG Encoder into any design.

As such, please note that the delivered folders may be missing the netlist file itself. Hence, the design can be fully connected/implemented but not simulated, nor synthesized into an FPGA bitstream.

The licensed version of the IP core consists of the same files, but with an added netlist, allowing bitstream generation without changes to the Qsys system implemented here.

Setting up the deliverables

In order to design JPEG systems with Intel Quartus' Qsys GUI tool, the accompanying files "jpeg[x]_encoder_hw.tcl" (AXI data interfaces), "jpeg[x]_encoder_st_hw.tcl" (AXI4-Stream data interfaces), and "jpeg[x]_encoder_stin_hw.tcl" (AXI and AXI4-Stream data interfaces) must be added to Intel's IP library by following these steps:

1. Locate the Intel Quartus SW installation folder (for example "C:\Program Files\Intel\14.0") .

2. Create a new sub-folder called "visengi" within Intel SW's "ip" subfolder (for example: "C:\Program Files\Intel\14.0\ip\visengi").

3. Copy the three ".tcl" files to the new "visengi" folder.

Instantiation

In order to instantiate the JPEGE IP core into a Qsys design, the following steps should be followed:

1. Open Intel Quartus SW, and then the project where the JPEGE is to be integrated.
2. Open the Qsys tool (Tools menu) and its .qsys project of choice (or create a new one).
3. In the IP Library, go to "DSP" and "Video and Image Processing"
4. The IP core will appear as "JPEG Encoder (AXI IO)" for the AXI only I/O interface, "JPEG Encoder (AXI4-ST IO)" for AXI4-Stream only I/O interfaces, and "JPEG Encoder (AXI4-ST In, AXI Out)" for AXI4-Stream pixel input and AXI data output interfaces
5. Select the preferred one and then click on the "Add" button.
6. The new instance will now appear in the design without any connections.

AXI vs AXI4-Stream Interfaces

The three JPEGE instances delivered feature the most common interfacing possibilities of the IP core's Data I/O interface.

Firstly, let's review the common interfaces:

- **Clock and reset:** the single clock (clk) and reset (rst) input ports are shared by all interfaces and internal logic. The reset is active-low Synchronous.

- **Configuration Interface (S_AXI):** AXI4-Lite slave with a 32 bits data interface and 12 bits addressing to control all the necessary parameters of encoding through a small Configuration register set. This is a low speed interface.

- **Interrupt Interface (JPEGEX_int_o):** A rising-edge interrupt is available, signaling when image compression has finished. Idle/busy status can also be checked through the Configuration register set.

The AXI3/4 interfaces contain DMA logic to enable connecting them directly to high speed buses towards external memory (or directly to a memory controller port) for data I/O.

On the other hand, AXI-4 Stream interfaces are meant usually to be connected as part of a pixel processing pipeline, for example.

The three different combinations of I/O buses available are:

1) **jpeg_encoder / jpegx_encoder** (JPEG Encoder AXI I/O):

The "M_AXI" bus (used to read **input pixels** and write the coded **JPG output**) is an **AXI3** Master, with a 32 bits data width (**little-endian**), embedded DMA engine for direct connection to a memory controller, and user-set addressing parameters through the Configuration register set. The "jpeg_encoder" is a Baseline JPEG Encoder (i.e. 24 bpp), whereas the "jpegx_encoder" is a Baseline and Extended Baseline (up to 36 bpp) encoder.

2) **jpeg_encoder_st / jpegx_encoder_st** (JPEG Encoder AXI4-ST I/O):

The **Pixel Input AXI4-Stream** Slave Interface is named "S_AXIS_PIX_IN" and can be connected to a Video IP AXI4-Stream Interface that feeds pixels in a row-wise manner (such as from an image sensor or video input).

Data width is 24 bits (for jpeg_encoder_st, JPEG Encoder Baseline) for 24bpp pixels. Or else data width is 40 bits (for jpegx_encoder_st, JPEG Encoder Extended), where pixels are LSB aligned as per AXI4-ST Video IP definition from Xilinx User Guide UG934. That is, bits [35:24] are for R/Cr component, bits [23:12] for B/Cb component, and bits [11:0] for G/Y component, as per Xilinx AXI4-Stream Video IP definition UG934.

If input is <12 bits per sample, the components are MSb aligned (example for 24bpp: R is at [35:28], G at [23:16], and B at [11:4]) and the LSbs of each color are to be 0-padded.

The Coded **JPG Output AXI4-Stream** Master Interface is named "M_AXIS_JPG_OUT". It outputs 32 bits words in a sequential manner (bytes in little endian order, as per AXI spec.). If they are written incrementally into a single file, the result is a .jpg file. Data width is 32 bits **little-endian** (i.e. 1st byte in .jpg file is the LSB, 4th byte is at the MSB). The last word of the .jpg file is padded if necessary (at its MSBs).

3) **jpeg_encoder_stin** / **jpegx_encoder_stin** (JPEG Encoder AXI4-ST In and AXI Out):

This third version features a mix of the above:

The **Pixel Input AXI4-Stream** Slave Interface is named "S_AXIS_PIX_IN" and is exactly the same as for jpeg_encoder_st (24 bits) / jpegx_encoder_st (40 bits) above.

The "M_AXI" bus (write only for the Coded **JPG Output**) is an **AXI3** Master, with a 32 bits data width (**little-endian**), embedded DMA engine for direct connection to a memory controller, and user-set addressing parameters through the Configuration register set.

Interfacing

The following interfacing scheme is recommended for maximum performance, since bottlenecks in the Data AXI interfaces are about the only way to slow down the JPEG Encoder.

In order to allow the IP core to maintain its constant pixel throughput, the data I/O AXI interface must be connected to a high speed slave with direct access to memory.

CPU/DDR Configuration:

In this **connection example** we will suppose a **Cyclone V SX** (or Arria V SX) FPGA, that is: an FPGA with embedded ARM CPUs.

> NOTE: the JPEGE IP core is fully autonomous, the use of a CPU in this example is just for convenience. It is only employed to configure the compression parameters (frame width/height, quality, DMA addresses, etc) through the AXI4-Lite interface. However, a soft-core CPU (such as Nios II) or even a simple FSM, can be used for the same purpose (on non-ARM enabled FPGAs).

The CPU is supposed to be the "Arria V/Cyclone V Hard Processor System" already at the top of the Qsys "System Contents" tab.

Double click on it to open the Parameters window and, on the **"FPGA Interfaces"** tab:

- Under the **"AXI Bridges"** section, make sure that the "Lightweight HPS-to-FPGA interface width" is set to "32-bit". This is where the AXI4-Lite Configuration interface (S_AXI) will go.

- Under the **"FPGA-to-HPS SDRAM Interface"** section, click the "+" button to add a new interface, select type "AXI-3" and width "32". This fast-speed AXI Slave interface will be used for the "AXI Data I/O Interface (M_AXI)", since it connects directly to DDR memory.

- Under the **"Interrupts"** section, make sure that there is a mark on the checkbox labeled "Enable FPGA-to-HPS Interrupts". This is where the JPEGE Interrupt output (JPEGEX_int_o) will connect to the CPU.

Close the Parameters window for the changes to take effect.

NOTE: On a non-ARM enabled FPGA, the S_AXI AXI4-Lite low speed bus should be connected to a soft-core CPU, or a suitable FSM, for configuration; whereas the AXI3 Data interface should be connected to a DDR Memory Controller port.

Interconnection:

Now all the necessary endpoints should be available in the Qsys "System Contents" tab. To properly connect the IP core these instructions should be followed.

To create the connections between ports/buses: click on the grayed out empty circles that make up the connections described, at the first column of the "System Contents" tab.

- The "reset_sink" Reset Input port must be connected to an active-low reset source.

  On Qsys, this could be the "clk_reset" Reset Output of a "Clock Source" block.

- The "clock_sink" Clock Input port must be connected to a rising-edge active clock source.

  On Qsys, this could be the "clk" Clock Output of a "Clock Source" block.

- The "JPEGEX_int_o" Interrupt Sender port must be connected to a rising-edge active interrupt receiver.

  On Qsys, this could be the "f2h_irq0" Interrupt Receiver of the "Arria V/Cyclone V Hard Processor System" block, the interrupt connections are done at the far-right side column of the "System Contents" tab.

- The "S_AXI" bus (used to access the JPEGE's Configuration Registers) is a standard AXI4-Lite interface of data width 32 bits.

  On Qsys, connect it to the low speed "h2f_lw_axi_master" bus of the "Arria V/Cyclone V Hard Processor System" block. Multiple components may be sharing this bus, which is fine.

- The "M_AXI" bus (used to read input pixels and write the coded JPG file) is a standard AXI3 interface of data width 32 bits, which can be directly connected to a memory controller, since it already embeds the necessary DMA engine.

  On Qsys, for maximum performance, it is recommended to connect it to the "f2h_sdram0_data" AXI slave, which is directly connected to the CPU's shared DDR Memory Controller.

NOTE: "f2h_sdram*_data" buses all connect the FPGA to the CPU's shared DDR memory controller. However, if there are other memory controllers on the FPGA side, they may be used instead, in order to ensure the maximum throughput for both the ARM CPU and JPEGE IP core.

Address Map:

Finally, click on the "Address Map" Qsys tab and find the following intersections in the table:

- **Row "jpeg[x]_encoder_*.S_AXI" and Column "hps_*.h2f_lw_axi_master"**: set here the assigned memory range to access the Configuration register set of the JPEGE IP core (remember that there is an added offset at run-time, which in the ARM on the SX FPGAs is 0xFF20_0000).

For example: typing "0x0001_1000" will make the address range become "0x0001_1000 – 0x0001_107f" (hence, accessible on SW at 0xFF21_1000 to 0xFF21_107F).

- **Row "hps_*.f2h_sdram0_data" and Column "jpeg[x]_encoder_*.M_AXI"**: set here the total memory range, by typing "0x0000_0000", which will become "0x0000_0000 – 0xFFFF_FFFF". The actual address range used by the JPEGE will be set in the Configuration register set.

To finalize, go to the File menu and Save, and then click on the button at the bottom-right labeled "Generate HDL....", accept the default settings and wait for the system to be validated and generated, if there are missing connections they will be reported.

When this is done, close the window and then click on the "Finish" button.

The system is ready!

For any question on how to best interface this IP core for your application,
please do not hesitate to send an email to info@visengi.com

